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10/788,420

03/01/2004

Richard Paul Brandwein JR.

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EXAMINER

LEE, SIU M

ART UNIT

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2611

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/788,420

Applicant(s)

BRANDWEIN, RICHARD PAUL

Examiner

Siu M. Lee

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-9 and 14-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-9 and 14-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-9 and 14-23 have been considered but are moot in view of the new ground(s) of rejection because of the amendment.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Oshima et al. (US 2001/0021144 A1).

(1) Regarding claim 1:

Oshima discloses a method of deriving a reference voltage for a data slicer comprising:

supplying a signal (MO BCA output from the reproduction signal output 255 and input to the LPF 943 in figure 14, figure 7 discloses a detail of reproduction signal output 255) to a filter (first low-pass filter 943a in figure 30) and filtering the signal (the first low-pass filter 943a filter the MO BCA signal);

amplifying the signal before the step of filtering the signal (before the MO BCA signal is output from the reproduction signal output 255, it is being amplified by a differential amplifier as shown in figure 7);

supplying the filtered signal to a comparator which comprises the data slicer (the filtered signal output from the first low-pass filter 943a is supply to the comparator 587c as shown in figure 30);

passing the signal prior to filtering through an RC circuit (the MO BCA signal is pass to the second low-pass filter 943b, wherein 943b is an RC circuit as shown in figure 30); and

using only the output of the RC circuit and no part of the filtered signal as the reference voltage for the comparator (the output of the second low-pass filter is use as the reference signal for the comparator 587c as shown in figure 30).

(2) Regarding claim 2:

Oshima et al. discloses wherein the filter is a low pass filter (the first low-pass filter 943a is a low-pass filter as shown in figure 30).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oshima et al. (US 2001/0021144 A1) in view of Mostov et al. (US 2006/0040630 A1).

(1) Regarding claim 3:

Oshima et al. discloses all the subject matter as discussed in claim 1 except wherein the data slicer forms part of a cascaded RF receiver system.

However, Mostov et al. discloses a radio frequency cascaded receiver system (receiver system in figure 4) that comprises a data slicer (data slicer 70 in figure 4).

It is desirable to have the data slicer form part of a radio frequency cascaded receiver because the data slicer can determine the received signal correctly. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Mostov et al. in the method of Oshima et al. to improve the integrity of the method.

(2) Regarding claim 4:

Oshima et al. discloses all the subject matter as discussed in claim 1 except wherein the signal is an IF (intermediate frequency) signal.

However, Mostov et al. wherein the signal is an IF (intermediate frequency) (Mixer 60 convert the radio signal received by the antenna 52 to intermediate frequency, paragraph 0054, lines 1-5).

It is desirable to convert the radio frequency received signal to an intermediate frequency received signal prior to be input to the slicer because it can remove a lot of interference in the radio frequency signal. Therefore, it would

have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Mostov et al. in the method of Oshima et al. to improve the performance of the method.

(3) Regarding claim 5:

Oshima et al. and Mostov et al. discloses all the subject matter as discuss in claims 1 and 4 except wherein the signal is an IF (intermediate frequency) signal and the frequency of the signal is up to about 4KHz.

However, it is pointed out in paragraph 0054 of Mostov et al. that the frequency of the intermediate frequency is determined by the frequency of the local oscillator 60 in figure 4. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention that the frequency of the local oscillator 60 can be set or adjust to a frequency that is up to about 4KHz so as to product an intermediate frequency signal with the frequency that is up to about 4KHz.

6. Claims 7, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oshima et al. (US 2001/0021144 A1) in view of Vilhonen et al. (US 6,972,633 B2).

Regarding claim 7, 8, and 9:

Oshima discloses all the subject matter as discussed in claim 1 except adjusting a value of a capacitor comprising the RC circuit or adjusting the value of a resistor of a RC circuit or adjusting the value of at least one of a resistor and

a capacitor of the RC circuit in order to modulate the reference voltage supplied to the comparator.

However, Vilhonen et al. discloses a method of adjusting the value of a capacitor of a RC filter circuit or adjusting the value of a resistor of a RC circuit or adjusting the value of at least one of a resistor and a capacitor of the RC circuit in order to modulate the reference voltage supplied to the comparator (RC-filter component includes at least one of a tunable resistor and a tunable capacitor, and wherein said calibrating component tunes said at least one RC-filter component of said loop-filter by changing at least the value of said tunable resistor and/or the value of said tunable capacitor of said at least one RC-filter component of said loop-filter, column 6, lines 1-8).

It is desirable to adjust the value of a capacitor of a RC filter circuit or adjusting the value of a resistor of a RC circuit or adjusting the value of at least one of a resistor and a capacitor of the RC circuit because it can calibrate the RC filter and provide flexibility for adjusting the characteristics of the filter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Vilhonen et al. in the method of Oshima et al. to increase the flexibility of the method.

7. Claims 14-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oshima et al. (US 2001/0021144 A1) in view of admitted prior art of the instant application (admitted prior art).

Oshima discloses a circuit comprising:

a filter (first low-pass filter 943a in figure 30) and a comparator (comparator 587c in figure 30) serially connected with a source (output of the photodetector 249 and 250 in figure 7), wherein the signal is amplified before being input into the filter (out put of the photodetector 249 and 250 is being amplified by a differential amplifier as shown in figure 7); and

a reference voltage circuit connected to the comparator (second low-pass filter 943b and light reference value setting portion 588 in figure 30) and configured to produce a comparator reference voltage (the value input to the negative input of the comparator 587c as shown in figure 30), the reference voltage circuit comprising a resistor (the resistor in the second low-pass filter 943b) and a capacitor (the capacitor in the second low-pass filter 943b), the resistor being connected to a point between the source and the filter so as to be responsive a signal which is being supplied to the filter in which the signal, prior to being filtered by the filter (the resistor in the second low-pass filter 943b is being connected to the input of the filter on one side as shown in figure 30) , is supplied as an signal input to the reference voltage circuit in order to produce the comparator reference voltage (the input signal to the filter (first low-pass filter 943a) is also input to the second low-pass filter 943b through the resistor in the second low-pass filter 943b).

Oshima et al. fails to disclose a source of an IF frequency signal for demodulation.

However, the admitted prior art discloses a source of an IF frequency signal for demodulation (IF signal output from the ASK/FSK switch 16 in figure 1).

It is desirable to provide an intermediate frequency signal for demodulation because it can remove interference in the received signal. Therefore, it would have been obvious to one ordinary skill in the art at the time of invention to employ the teaching of the admitted prior art in the circuit of Oshima et al. to improve the performance of the circuit.

(2) Regarding claim 15:

The admitted prior art discloses that the source of the IF frequency signal comprises an ASK/FSK switch (IF signal output from the ASK/FSK switch 16 in figure 1).

(3) Regarding claim 16:

The admitted prior art discloses that the wherein the source of an IF frequency signal, filter and comparator serially connected with the source, comprise elements of an internal stage of a chip (figure 1 discloses that the ASK/FSK, the low pass filter 14 and the comparator 18 is an internal stage of a chip 10 PLL (phase locked loop IC), paragraph 0004-0005).

(4) Regarding claim 17:

Oshima et al. discloses a circuit comprising:

a filter (first low-pass filter 943a in figure 30) and a comparator (comparator 587c in figure 30) serially connected with a source (output of the photodetector 249 and 250 in figure 7);

a reference voltage circuit connected to the comparator (second low-pass filter 943b and light reference value setting portion 588 in figure 30) and configured to produce a comparator reference voltage (the value input to the negative input of the comparator 587c as shown in figure 30), the reference voltage circuit comprising a resistor (the resistor in the second low-pass filter 943b) and a capacitor (the capacitor in the second low-pass filter 943b), the resistor being connected to a point between the source and the filter so as to be responsive a signal which is being supplied to the filter in which the signal, prior to being filtered by the filter (the resistor in the second low-pass filter 943b is being connected to the input of the filter on one side as shown in figure 30) , is supplied as an signal input to the reference voltage circuit in order to produce the comparator reference voltage (the input signal to the filter (first low-pass filter 943a) is also input to the second low-pass filter 943b through the resistor in the second low-pass filter 943b).

Oshima et al. fails to disclose a source of an IF frequency signal for demodulation and wherein the source of an IF frequency signal, filter and comparator serially connected with the source, comprise the element of an internal stage of a chip and the resistor of the reference voltage circuit is an internal element of the chip.

However, the admitted prior art discloses a source of IF frequency signal for demodulation (the IF frequency signal output from the ASK/FSK switch 16 in figure 1) and wherein the source of an IF frequency signal, filter and comparator serially connected with the source (ASK/FSK switch 16, low pass filter 14 and

comparator 18 are serially connected together as shown in figure 1) comprise elements of an internal stage of a chip (the PLL IC 10 in figure 1 comprises the ASK/FSK switch 16, low pass filter 14 and comparator 18 are serially connected together as shown in figure 1) and the resistor of the reference voltage circuit is an internal element of the chip (R3 of the RC circuit is an internal element of the PLL IC 10 in figure 1) (it is obvious that the resistor of the RC circuit be included in the internal stage of a chip).

It is desirable to have a source of an IF frequency signal for demodulation and wherein the source of an IF frequency signal, filter and comparator serially connected with the source, comprise the element of an internal stage of a chip because can it can remove interference in the received signal; and by interpreting the element in an internal stage of a chip, it can reduce the circuit size and reduce power consumption of the circuit. Therefore, it would have been obvious to one ordinary skill in the art at the time of invention to employ the teaching of the admitted prior art in the circuit of Oshima et al. to improve the performance of the circuit and reduce the power consumption of the circuit.

(5) Regarding claim 18:

Oshima et al. and the admitted prior art disclose all the subject matter as discussed in claim 16 except wherein the capacitor of the reference voltage circuit comprise parts of an external stage of the chip.

Although Oshima et al. in view of the admitted prior art do not specifically disclose wherein the resistance and the capacitor of the reference voltage circuit comprise parts of an external stage of the chip, such limitation are merely a

matter of design choice and would have been obvious in the circuit of Oshima et al.. Oshima et al. in view of the admitted prior art teaches the circuit of claim 16. The limitation in claim 18 do not define a patentably distinct invention over Oshima et al. in view of the admitted prior art since both invention as a whole is the same. Therefore, the capacitor of the reference voltage circuit comprises parts of an external stage of the chip would have been a matter of obvious design choice to one of ordinary skill in the art.

(6) Regarding claim 19:

Oshima et al. and the admitted prior art disclose all the subject matter as discussed in claim 16 except wherein the resistance and the capacitor of the reference voltage circuit comprise parts of an external stage of the chip.

Although Oshima et al. in view of the admitted prior art do not specifically disclose wherein the resistance and the capacitor of the reference voltage circuit comprise parts of an external stage of the chip, such limitation are merely a matter of design choice and would have been obvious in the circuit of Oshima et al.. Oshima et al. in view of the admitted prior art teaches the circuit of claim 16. The limitation in claim 19 does not define a patentably distinct invention over Oshima et al. in view of the admitted prior art since both invention as a whole is the same. Therefore, the resistor and the capacitor of the reference voltage circuit comprises parts of an external stage of the chip would have been a matter of obvious design choice to one of ordinary skill in the art.

(7) Regarding claim 20:

Oshima discloses a circuit comprising:

a filter (first low-pass filter 943a in figure 30) and a comparator (comparator 587c in figure 30) serially connected with a source (output of the photodetector 249 and 250 in figure 7), wherein the signal is amplified before being input into the filter (out put of the photodetector 249 and 250 is being amplified by a differential amplifier as shown in figure 7); and

a reference voltage circuit connected to the comparator (second low-pass filter 943b and light reference value setting portion 588 in figure 30 in connected to the comparator 587c) and configured to respond to a signal having a component which is comparable with a component filtered by the filter (the output of the first low-pass filter 943a) in which the signal, prior to being filter by the filter, is supplied as an only signal input to the reference voltage circuit ((the input signal to the filter (first low-pass filter 943a) is also input to the second low-pass filter 943b through the resistor in the second low-pass filter 943b) in order to produce the comparator reference voltage.

Oshima et al. fails to disclose a source of an IF frequency signal for demodulation.

However, the admitted prior art discloses a source of an IF frequency signal for demodulation (IF signal output from the ASK/FSK switch 16 in figure 1).

It is desirable to provide an intermediate frequency signal for demodulation because it can remove interference in the received signal.

Therefore, it would have been obvious to one ordinary skill in the art at the time of invention to employ the teaching of the admitted prior art in the circuit of Oshima et al. to improve the performance of the circuit.

(8) Regarding claim 21:

The prior art of the instant application discloses wherein the circuit forms part of a wireless communication device (as it states in paragraph 0002, the present invention relates generally to a receiver circuit for use in devices such as keyless entry receiver circuit, it indicates that the prior art discloses in figure 1 is also generally related to the same kind of application, which is a wireless communication device).

It is desirable to for the circuit to form part of a wireless communication device because it allows the receiver to be produced economically (paragraph 0002, lines 6-7). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of the admitted prior art in the circuit of Oshima et al. to reduce the production cost.

(17) Regarding claim 22:

The prior art of the instant application further discloses wherein the wireless communication device comprises a keyless entry system for an automotive vehicle (for the same reason as states in claim 21 above, it is obvious to one of ordinary skill in the art at the time of invention to apply the keyless entry receiver circuit for an automotive vehicle).

(18) Regarding claim 23:

The prior art of the instant application discloses wherein the wireless communication device comprises a tire pressure monitoring system for an automotive vehicle (for the same reason as states in claim 21 above, it is obvious

to one of ordinary skill in the art at the time of invention to apply the keyless entry receiver circuit for a tire pressure monitor system for an automotive vehicle).

### ***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIU M. LEE whose telephone number is (571)270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax

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phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M Lee  
Examiner  
Art Unit 2611  
2/25/2008

  
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